

60. (Added Claim) A semiconductor manufacturing system as recited in claim 59 further comprising:

an inspection tool attached to one of the facets of the wafer handling chamber, wherein the inspection tool reviews semiconductor wafers for defects.

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61. (Added Claim) A semiconductor manufacturing system as recited in claim 60 wherein the optical inspection tool is a modular optical inspection system that includes

a plurality of modular inspection subsystems each configured to detect defects on a portion of a semiconductor wafer;

a mechanism for moving at least one of the semiconductor wafer and the plurality of modular inspection subsystems with respect to one another; and

a master processor configured to process data delivered from at least some of the modular inspection subsystems, wherein a first one of the plurality of modular inspection subsystems includes a local processor configured to process data collected by the first modular inspection subsystem.

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62. (Added Claim) A semiconductor manufacturing system as recited in claim 59 wherein the metrology tool is an ellipsometer configured to measure the thickness of a layer on the surface of the semiconductor wafer.

63. (Added Claim) A semiconductor manufacturing system as recited in claim 59 wherein at least one of the process tools is a type of tool selected from the group consisting of a CVD reactor, an etcher, and a stripper.

64. (Added Claim) A semiconductor manufacturing system as recited in claim 59 further comprising:

a wafer storage cassette that is attached to one of the facets on the wafer handling chamber.

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65. (Added Claim) A method of manufacturing a semiconductor wafer comprising:
providing a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;

providing a plurality of wafer processing tools, each of the tools being attached to a respective facet on the wafer handling chamber;

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and

providing a metrology tool attached to one of the facets of the wafer handling chamber, wherein the metrology tool measures physical parameters on semiconductor wafers;
transferring the semiconductor wafer from one of the plurality of wafer processing tools to the metrology tool;
measuring the dimension of at least one feature on the semiconductor wafer with the metrology tool.

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66. (Added Claim) A method of manufacturing a semiconductor wafer as recited in claim 65 further comprising:

providing an inspection tool attached to one of the facets of the wafer handling chamber, wherein the inspection tool reviews semiconductor wafers for defects;
transferring the semiconductor wafer from the metrology tool or one of the wafer processing tools to the inspection tool; and
inspecting the semiconductor wafer for defects using the inspection tool.

REMARKS

In the Office Action, claims 1, 4-6, 9, 11, 13-22 and 43-58 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Morioka et al. (U.S. Patent No. 5,274,434) taken with Morioka et al. (U.S. Patent No. 5,463,459) and Yamamoto et al. (U.S. Patent No. 5,623,340), and also with Levy (U.S. Patent No. 5,465,154).

Claims 1, 5-6 and 9, 13-22, and 43-58 have been canceled. New claims 59-66 have been added. Claims 59-66 are now pending.

Independent claims 59 and 65 pertain to systems wherein a semiconductor manufacturing system includes a wafer handling chamber wherein a metrology tool is attached to a facet of the chamber. Direct attachment of the metrology tool to the chamber is advantageous in that the metrology tool can be used immediately after a wafer processing step that occurs in a similarly attached wafer processing tool. In contrast, Morioka et al. (U.S. Patent No. 5,274,434), Morioka et al. (U.S. Patent No. 5,463,459), Yamamoto et al. (U.S. Patent No. 5,623,340), and Levy (U.S. Patent No. 5,465,154) do not disclose a metrology tool that is directly attached to a facet of a wafer handling chamber. Specifically, FIG. 22 of Morioka et al. ('434) describes inspection systems that are attached to a process chamber. However, these inspection systems are not